# NEIL MAMMEN
# TENTMAKER SYSTEMS CONSULTING GROUP
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## INNOVATOR, LEAN STARTUP, ARCHITECT, HW ENGINEER & TEAM MOTIVATOR

**Hands on System/Board/Chip Architect and Technologist, Chip & New Product Specification and Architecture, Board/System/Product/FPGA Architecture & Design. Technical Marketing and Evangelism assistance. Product Applications Boards, Reference Designs and Support. RTL, ASIC Verification and Validation boards and FPGAs.**

# Some Accomplishments and Skills:

Over 18 Patents (applied, granted or pending) in various fields (assigned to customer or company e.g. Intel, Dolby, Luminous, Xalted etc.).

Skilled (with practical experience) in taking concepts, algorithms and *customer* requirements and creating a manufacturable System Architecture or ASIC architecture; and then driving it through design to completion.

Skilled at presenting and gaining customer (and VC) confidence and loyalty through training, presentations and interaction.

Long term relationships with manufacturing and assembly facilities for quick turn boards in US and medium turn and production in China.

Joined Dolby on request to bring a fully functional HDR monitor demo to CES in 3 months. Internal group wanted 7 months to architect, design and have a PCB ready for CES with their team of 8. Their delivery date was going to be March, CES is beginning of January. Joined end of Sept, and single handedly architected, designed, leveraged long term relationships to layout, fab, assemble and have boards ready for system level and firmware/Verilog debug by the end of November. Made CES with fully functional system, 2 weeks ahead of time.

To prove viability, went from white board drawings to functioning Apollo Dolby Vision™ proof of concept monitor in 6 weeks.

Sole Hardware Designer of every single one of Dolby's Dolby Vision® monitors.

Experience with ASIC Verification targeting very large FPGAs including schematic design, power design, high speed Serdes and DDR interface.

Experienced Video Systems Architect.

High Speed Serdes FPGA and board design.

Experienced High Density and high-speed FPGA Architecture and Verilog Design. Altera and Xilinx.

Experienced Systems and Board Architecture, Design, Bringup Debug etc.

Experienced Chip/ASIC Architect.

Helped raise over $70M in VC and Investment Funding for Systems Company as CTO.

Co-founded and raised $15M VC funding for startup ASIC company.

Managed teams of engineers to bring complex systems and products to market.

Conceived and architected the world's first ***Clear Channel*** 40G Layers 2-4 Network Processor ASIC multichip set. Design scales down to provide a Clear Channel 10G Network Processor. Took design through funding, recruiting, Micro-Architecture and a functioning cycle accurate C-Model. Authored and applied for 16 patents in multiple areas including Memory Bandwidth, Statistics Collection, Network Processing, Traffic Shaping etc. This chip was on schedule to be released in 2003. But in 2002, our VC's said we were 10 years ahead of the market and opted to shut us down.

VC's suggested we pivot to SAN product. So, within 2 months architected a 32G SAN switch chipset for company's new direction. Two new patents started but not filed due to company closure.

Co-designed, Product Planned and Specified the world's first ever MPEG1 layer 2 player chip in 1992 (precursor to MP3)

Helped Samsung and Panasonic design and implement their first ever MPEG players (pre-DVD) between 1992-1994.

Architected large 200+ card Optical DSL system as a consultant. Co-author of the patent issued on my Architecture.

Called in for Emergency Consulting. Prior 4-man team had taken 6 months and hadn't been able to get high speed MAC design to work. Threw away entire prior architecture and started design from scratch. Single handedly re-architected, designed, implemented and debugged and reliability tested in 6 weeks, a complete 1G Backplane Proprietary IP Packet MAC in a space and speed limited FPGA at 125MHz for a Metropolitan Area Network (MAN) implementation. This allowed company to show working systems to customers on schedule. Created 8 versions of this FPGA which were used in every one of the company's Networking blades. Subsequently, expanded the design to provide a 2.5G MAC in an FPGA with internal speeds of 156MHz DDR. This allowed company to ship their 2.5G MAN products ahead of anyone else.

Co-author of multiple Luminous Networks patents in MAN field relating to Traffic Shaping and Reliability.

Designed and implemented FPGAs incorporating, I2S audio, VESA VIP and SPDIF standards.

Architected an OC192, Video Aware IP Network Processor. (Preliminary Specifications and Block level). Startup company raised money partly on this architecture.

Responsible for Engineering Department of 40 engineers and technicians and documentation, taken over from old VP of Engineering who was discharged.

Proposed and architected a MPEG2/ATM Multi-Re-multiplexer System solution for major European Telco.

Proposed, architected, designed and submitted RFP for the *winning* SouthWestern Bell MPEG2 Deployment System solution. System was manufactured and deployed for testing.

Proposed, architected, designed and submitted RFP for the *winning* Hong Kong Jockey Club MPEG2 Deployment System solution, competed and won out against IBM (we were using their own chipset against them).

Proposed, architected and designed the *winning* NORTEL DV-45 MPEG2 Codec contract.

Came up with the concept and wrote initial product requirements & specs of the iCompression MPEG2 codec chip. The worlds first single chip Audio/Video Data Encoder and TS Mux chip. Conceived of and identified the strategic need for a single chip multi-featured codec and was instrumental in locating the founders and helped promote and finance the company through NUKO Information Systems. iCompression was later sold for $500M to Globespan.

Within 4 months of joining start up (unpaid), recruited 3 engineers (also unpaid), architected, designed, laid out, manufactured and debugged 2 new boards and 2 reference designs, to prototype a 7-channel real time MPEG 2 encoder and decoder to demonstrate the *world's very first* multi-channel MPEG 2 codec to work over DS3. Thus, became the designer of the very first MPEG Video over DS2 and 7 Video Streams over DS3. Our first demo was to send live video streams from Stanford University to NAB in Las Vegas in 1994.

Architect and primary FPGA, Board and System designer of the NUKO Highlander MPEG 2 System. Includes the MPEG 2 Multifunction Transport Stream Multiplexer and the NUKO Highlander MPEG 2 Multifunction Decoder. System includes multiple redundancy utilizing on board Alarms, redundancy SW, SNMP, GUIs etc.

Creator of the "Mammen" VME Hotswap Methodology, before there was a VME64 Hotswap. Used successfully and reliably in the NUKO Highlander System with 0 failures in 4 years. Units in use were still running 8 years later.

Architect and primary designer of the NUKO IBM MPEG 2 Encoder solution.

Co-Architect of the Multistream ATM Trunking Multiplexer and DeMultiplexer. Allowed the use of up to 9/36 MPEG 2 multi-rate bandwidth streams to work on OC-3 lines over ATM framing, with multiple redundancy.

Sole applications engineer for the *world's first* C-Cube MPEG 1, "1+" & 2 Encoder chipset and microcode. Supported over 25 customers (simultaneously) in enabling them all to come to market with Real Time MPEG 1, "1+" and 2 Encoders. At one point in time, of the 17 production MPEG encoders available in the world, had helped design and debug 15 of them.

Helped specify new product features and requirement for an MPEG Audio encoder vendor (that I was unaffiliated with but needed for a product of my own). This audio encoder module proved to be an enormous success for that company (Atlanta DSP).

As a newly hired applications engineer at C-Cube, within 2 weeks, single handedly discovered and designed work around for an interface flaw in primary product that 2 previous applications engineers and the chip's own design engineer had spent 4 months trying to find. Fixing this problem resurrected a key design with a key customer (Philips Semiconductor, worth $3M) and allowed us to correct our Technical Manuals. Problem detection included having to evaluate

original VLSI design and state machines and then design a programmable logic device to compensate for the bug.

Through my direct intervention, effort and management, resurrected and maintained a critical NRE account worth over millions just when the company thought we were going to lose it all (C-Cube & Panasonic).

Came up with an innovative work-around to help crucial customer (Cable Labs) get to market ahead of schedule before critical inverse telecine microcode was available.

Debugged new chip revision to discover critical temperature issue, which further explained other failures to date. This was a bug that had plagued the company before I attacked the problem. (Panasonic).

Product Planning for *world's first* LSI Logic Audio MPEG 1 Decoder Single Chip. Defined features set, designed Evaluation board and wrote software. Provided Technical Seminars for Customers and FAEs. Chip forecasted over $10 Million in sales within the first 2 years. Wrote Technical Manual.

Applications support for LSI's first generation CCITT H.261 video chipset. Joined division and within a month, implemented a last-minute mask fix on the existing chipset to make it reliable. Included recommending a new spin of the old chipset to correct system I/F problems and bugs.

In 4 months started up and established a fully functional applications group to support new SPARC RISC chipset, SparKIT. Hired and trained 9 engineers. Developed evaluation boards for customer training and chip debug, installed Customer Hotline, databases, started FAE magazine, FAEdback, etc. COMDEX shows, developed and produced customer training seminars around the world.

As manager of the SPARC Applications Department was responsible for design and manufacture of boards, chip specifications, product planning and debug of chips for the SparKIT-25 and 40, IU, FPU, MMU and Peripherals to the Mbus and SBus. Included the assist of debug and porting of SUN OS 4.1 to the new MMU and peripherals. Other support products included SUN OS and the original chips in the SUN SPARCstation 1, 1+, 2, IPC etc. and their clones. Responsibilities included SPARC International compliance test suits. Responsible for training FAEs and sales force on our chipsets as well as competitor's chips.

Established, stocked and managed fully functional lab for 3 divisions, (SPARC, MIPS & DSP), included set up for customer demos as well as setups for customer board debugging and support.

Responsible for production and content (with Tech Pubs) of entire line of SPARC Technical Manuals and Data Sheets for above products. We produced over 20 publications of which 11 were Technical Manuals.

Worked with 12 PC manufacturers to enable them to create the first SUN SST1 (SPARCstation 1) and SST1+ clones.

Taught RISC Microprocessor/System technical seminars around the world in cooperation with SUN Microsystems.

Set up documentation procedure to allow the sign-off, control, production and update of technical manuals, errata and appnotes through-out the world. Included the "FASTfax" system to

immediately getting critical applications and errata information to customers without having the delay of going to Tech Pubs. System was later standardized and adopted by other divisions.

With engineering partner, discovered only way to correct more than $100,000 worth of already manufactured TAXIchip™ parts. Saving inventory, customer loyalty, future sales, and company's public image.

Primary, world-wide Application Engineer for the AMD TAXIchip™, 125 MHz high speed, point to point I/F chipset. Wrote the TAXIchip™ Technical Manual, designed the MINIcab™ and TAXIcab™ boards. Wrote specs, assisted customers in their designs and designed future products. Taught TAXIchip™ seminars around the US. The TAXIchip is currently an industry standard of sorts.

Implementer of the world's first digitized video Transmission over Fiber: In 45 days designed an NTSC high speed 2 Km fiber optic video digitizing board for key customers, a major show, seminars and engineering publications, resulting in major sales and publicity. This system was used in a slightly modified form by various customers for security cameras as well as by airline companies for personal video entertainment at your seat.
Above system was tapped by the US Military and DOD to create the first FOGMs (Fiber Optic Guided Missiles). Since I was not a US Citizen at the time and did not have any security clearances, I was only allowed to provide generic support, i.e. they would ask me lots of questions only a few of which were the problem they actually were trying to fix.

Authored and gave TAXIchip™ seminars given throughout the US.

Coordinated and organized transfer of manufacturing between wafer fabrication areas. Saved company over $1,000,000 in fab operational costs.

Came up with innovative solution working with a vendor at a show. Vendor only had one demo temperature test chuck that our test engineers needed to test chips. Testing, assembly and shipment of this critical chip was halted due to the need for this chuck. Figured out a way for vendor to keep showing it at the show and let us use it for testing.

# Other Skills and Tools

Xilinx, Altera, C, various Schematic Entry and FPGA development packages, Verilog, StateCAD, Synplicity, ModelSim, VCS, Silos III, OrCAD, PCAD, Renoir.

# Other Activities

Motivational Speaking, Training individuals to give effective presentations, Training lay people to be effective speakers and preachers, Video Editing and Production, Audio Production

"MOD Night" Once a year for about 10 years used to lead, coordinate and manage an extracurricular activity involving over 120 volunteers and over 380 Junior High kids in a two night "Outward Bound" style Night Game activity spread out around the Santa Cruz, CA and Portland, OR mountains.

Mentoring youth and younger engineers.

# Quick Architecture and Design Summary

**Boards, Systems and FPGAs. Unless indicated, includes Design, Architecture, FW, SW, Systems Architecture and support. Covers some of the items mentioned above as well:**

TAXIcab : TAXIchip Circuit Application Board: First high speed Serdes
TAXIvideo : TAXIchip Video Transmission Board: First Ever Demo of Digitized Video over Optical Fiber
Saavik 1 & 2: LSI Logic MPEG 2 over DS2 ISA Decoder board.
Spock I : 9U VME Audio/Video Multiplexing board
Spock III : 8 input Transport Stream Multiplexing board designed using FPGAs.
Sarek III : 9U VME C-Cube MPEG 2 Encoder board. Multiple FPGAs.
DV-MPEG : Hot-swappable NORTEL Chassis Codec System (6U) consisting of the 4 boards below.
Riker : IBM MPEG 2 Encoder board
William : Hot-swap NORTEL Motherboard for above Encoder.
Troi : C-Cube Decoder Board
Deanna : Hot-swap NORTEL Motherboard for above Decoder.
Atlas : 9U VME Fully Redundant mother board for a full featured Codec
Sammy : 9U VME Video Input, Audio Encoder, MPEG TS muxer board
Uhura : 9U VME 9 channel ATM TS multiplexer over OC3c or DS3 (Specifications and co-architect)
Aruhu : 9U VME 9/36 channel ATM TS demultiplexer over OC3c or DS3 (Specifications and co-architect)
Highlander : Multi-Redundant 44/40 U chassis 9 channel 9U Codec system
iCompression Single Chip Encoder
: Primary Systems level definition for the iCompression Single Chip MPEG 2 Encoder, also initiated the founding of iCompression and gave them $2M startup to provide me with a substitute for the C-Cube encoder.
Picard : iCompression Encoder PCI board.
ReMuxer : Architect of the MPEG2/ATM Multi-Re-multiplexer System and Chassis
TPM1 FPGA: DIVA Systems Transport Processor Module,
Completely re-architected and redesigned their Transport Processor FPGA.
TPMII : DIVA Systems Transport Processor Board II.
Architected the second generation of the DIVA board for Video on Demand.
Architected and designed the core FPGA, the M4SPROC, a 4 stream MPEG TS processor.
TPMtester : DIVA Systems Tester board.
Architected, designed, debugged this large test board with multiple connectors and connections to allow a fast test and bring-up environment for the DIVA TPMII boards.
DVB2MII : Luminous Video TS DVB to Ethernet Board including all FPGAs. Implemented a module to convert and reconvert Video TS to IP over Ethernet to allow it to be transmitted over any 100baseT network. Board and FPGA was used for demo systems at shows and was used to capture a critical investment.
LMAC 1G :Luminous Backplane MAC FPGA. Multiple flavors of this FGPA were shipped in all Luminous Products, with multiple per card and upto 6 on the Switch Card.
LMAC 2.5G: Luminous Backplane MAC FPGA. This FPGA was shipped in all 2.5G Luminous products.
VIP Interface: FPGA that interfaces MPEG TS and I2S and SPDIF to a VESAVIP bus.

PCI to HPI bus interface: FPGA that interfaces PCI to local bus. Includes CCIR656 Interface to PCI, interface ensures ability to preview with VCR FF and REW inputs.
PCIexpress Northstar III: Implementation of Xilinx core for proof of concept. Done in 12 weeks to demo with working video.
PCIexpress FPGA/ASIC Verification suite of boards: Validation of PCIe and Video ASIC RTL in FPGA
PCIexpress ASIC board: Validation board for PCIe ASIC chip with video.
Multiple other PCIe designs.
Dolby HDR and Dolby Vision Boards (partial list): Contrast, Phoenix, Lanai, Pulsar, Pulsar II, Maui, Apollo (numerous other projects in the AR/VR field still confidential).
**(Multiple other Consulting designs not listed as some are confidential).**

# Background Summary

**Tentmaker Systems Consulting: 2018**

- T3, Dolby Labs, Light Field Labs

**Dolby Labs**: **2008-2018**

**- Senior Staff Engineer.** Was Consulting, joined to help Dolby to deliver an emergency project for the CES Show. Internal group wanted 7 months to architect, design and have a PCB ready for CES with a team of 8. Their delivery date was going to be March. Joined end of Sept, and single handedly had boards ready for system level debug by the end of Nov. Made CES with functional system 2 weeks ahead of time. Went on to design over 30 PCBS for multiple projects. HW architect and designer for every Dolby Vision monitor made by Dolby and all but two Dolby HDR monitors. Designed the Pulsar Monitors that became the platform for the development of Dolby Vision.
Coauthor of 5 Dolby Patents.

**Tentmaker Systems Consulting: 2002-2008**

- Xilinx, JDSU, Brilliant, nVidia, Netlogic Microsystems, Mentor Graphics, Reliancy, BBNC, Stream Processors, Philips Semiconductor (various groups within Philips)/NXP, WIS Technologies (various fill in roles within WIS), DataRobotics, Audience, Varian Medical Systems etc.

**Propulsion Networks: 2001-2002**

**- Co-Founder, Chief Architect and VP of Technology**.
Conceived, Proposed, Defined and Architected a Metro/Core Router 40G/10G Network Processor. Raised $15M in VC funding. All schedules met. Fully functional gate level C-Model demonstrated. Received lots of customer enthusiasm and validation.

Applied for about 16 patents all currently owned by Intel now.
Due to delayed market for 40G Network Processors, the VC's opted to close down the company and sell off the IP.

**Luminous Networks: 1999-2001**

- Was consulting - joined at the request of the CTO and CEO
- **Principal Architect, Office of the CTO**
- **Director, ASIC Design.**
  Requested by the CEO to take over the ASIC group.
  Did so till I was able to hire someone to replace me.
  Co-Author of 2 Luminous patents
- Left to start my own company as per my prior agreement with the CTO & CEO.

**Bay Micro Systems: 1998-2000**

- Co-founder.
- Helped raise $3M in Venture Funding

**Tentmaker Systems Consulting:**

- Xalted IP Networks
- Luminous Networks
- Azanda Microsystems
- DIVA Systems
- Cradle Technologies
- Pulsent Technologies
- Dynachip
- ShivaSAT
- ADC Communications

**NUKO Information Systems:**

Helped raise $70M in funding based on my architecture
- **Chief Technology Officer & VP of Engineering**
- **Chief Technology Officer**
- **Chief Technologist**
- **Joined as Director of Engineering and cofounder**

**Tentmaker Systems Consulting:**

- NUKO Information Systems

**C-Cube Microsystems:**

- **Manager,** System Design and Applications
- **Senior Staff Applications Engineer**, System Design

Helped design the very first Samsung and Matsushita DVD players in 1993.

**LSI Logic:**

- **Senior Staff Member,** Applications, DSP Division.
- **Manager, SPARC Applications Engineering**

**Tentmaker Systems Design:** -PC based Video Editor System Design

**Advanced Micro Devices:**

**- Senior Product Planning and Applications/Strategic Development Engr**, High Speed Serial Interface/Optical/Networking Development Group.
Designed the very first ever digitized video over fiber transmission as a demo (with Eugen Gershon).
- Product Engineer, Microprocessors Division.

**Spectra-Physics:**

**- R&D Associate Engineer,** Laser System Division (Eugene, Oregon) Electronic Design and Interface.

**UC Berkeley Extension:**

- Taught Digital Logic Design and Digital Logic Design Lab. Highly ranked by Students Surveys.

# Education

- **MSEE**, Computer Engineering and Solid-State Physics, Oregon State University.
Master's Degree Thesis: A Bit Slice Microprocessor Learning System

- **BSEE**, Electrical Engineering and Computer Engineering, Oregon State University.

# Societies and Awards

- President, Tau Beta Pi OR Alpha Chapter
- Eta Kappa Nu
- Chairman of IEEE Student Organization, OSU
- Teaching Assistant of the Year Award, OSU (Electrical Engineering Department Students)
- Wyle/EE Times American By Design Contest, 1st Place Design Winner for Digital Devices.
- Wyle/EE Times Idea Quest Grand Prize Winner. Winner of the Saturn EV1 Electric Vehicle.
- NUKO Summit Award

# Some Business and Personal References:

**Jayshree Ullal,**
CEO, Arista Networks

**Bob Kondamoori,**
Previous Position: CEO and Chairman of the board, NUKO Information Systems

**Ram Kedlaya,**
Previous Position: VP Business Development, NUKO Information Systems

**Additional References Available on Request**

# Partial list of Patents (applied, pending or granted)

**Systems and Methods for Display Systems Having Improved Power Profiles**

**Publication number:** 20140307011
**Abstract:** Techniques are provided to provide various pulse width modulation (PWM) schemes to embodiments of dual modulator display systems that may comprise a backlight of individually addressable and controllable light emitters. The backlight provides illumination to a light modulator for further conditioning of the light to be presented to a viewer. The backlight may be striped and each stripe is assigned a PWM scheme that effectively increases the bit depth of the controller for each stripe. The display system may allow a better matching of PWM periods to LCD frame rates to reduce visual artifacts. In another embodiment, the display system may detect a small bright feature to be rendered in the image data and, with a pre-assignment of light emitters to different partitions, the backlight controller may drive a subset of the light emitters according to the partitions.
**Type:** Application
**Filed:** November 7, 2012
**Publication date:** October 16, 2014
**Applicant:** DOLBY LABORATORIES LICENSING CORPORATION
**Inventors:** Ajit Ninan, Qifan Huang, Greg Maturi, Neil Mammen, James Kronrod

**Variable flower display backlight system**

**Patent number:** 8836736
**Abstract:** Techniques for using variable flower assemblies to control light leakage between designated portions of light-emitting elements are provided. In some embodiments, a variable flower assembly (100) comprises a plurality of light-transmissive segments (102-1, 102-2, . . . , 102-6) each may be electronically set to a different light-transparency level. The variable flower assembly substantially forms a tube around a light-emitting element (104) mounted on a first plane. A first edge of each of the light-transmissive segments collectively surrounds the light-emitting element on a second plane substantially parallel to the first plane. A second opposing edge of each of the light-transmissive segments collectively forms an opening of the tube. In some embodiments, a reflective assembly (120) which reflectance level is electronically controllable may surround the variable flower assembly.
**Type:** Grant
**Filed:** October 13, 2010
**Date of Patent:** September 16, 2014
**Assignee:** Dolby Laboratories Licensing Corporation
**Inventors:** Neil Mammen, Ashley Penna, Ajit Ninan

**Method and apparatus for using multiple network processors to achieve higher performance networking applications**

**Patent number:** 7606248
**Abstract:** An apparatus is described having a plurality of network processors that identify, for each of a plurality of packets, which multidimensional queue from amongst a plurality of multidimensional queues that each one of the plurality of packets should be enqueued into. Each of the network processors is able to identify a particular multidimensional queue for a different one of the plurality of packets.
**Type:** Grant

**Filed:** May 10, 2002
**Date of Patent:** October 20, 2009
**Assignee:** Altera Corporation
**Inventors:** Greg Maturi, Neil Mammen, Sagar Edara, Mammen Thomas

### Method of policing network traffic

**Patent number:** 7593334
**Abstract:** According to one embodiment, a method of regulating traffic at a network hardware machine is disclosed. The method includes receiving a data packet, calculating a time stamp difference value, determining whether a maximum token bucket value has been exceeded by the time stamp difference value and determining whether there are enough tokens to transmit the packet.
**Type:** Grant
**Filed:** May 20, 2002
**Date of Patent:** September 22, 2009
**Assignee:** Altera Corporation
**Inventors:** Neil Mammen, Sanjay Agarwal

### Apparatus and method for queuing flow management between input, intermediate and output queues

**Patent number:** 7339943
**Abstract:** An apparatus is described that includes a plurality of queuing paths. Each of the queuing paths further comprises an input queue, an intermediate queue and an output queue. The input queue has an output coupled to an input of the intermediate queue and the input of the output queue. The intermediate queue has an output coupled to the input of the output queue. The intermediate queue receives data units from the input queue if a state of the input queue has reached a threshold. The output queue receives data units from the intermediate queue if the intermediate queue has data units. The output queue receives data units from the input queue if the intermediate queue does not have data units.
**Type:** Grant
**Filed:** May 10, 2002
**Date of Patent:** March 4, 2008
**Assignee:** Altera Corporation
**Inventors:** Neil Mammen, Greg Maturi, Mammen Thomas

### Mechanism for distributing statistics across multiple elements

**Patent number:** 7336669
**Abstract:** According to one embodiment, a network is disclosed. The network includes a source device, a networking hardware machine coupled to the source device, and a destination device coupled to the networking hardware machine. The networking hardware machine receives data packets from the source device and distributes statistics data corresponding to the data packets among multiple internal memory devices.
**Type:** Grant
**Filed:** May 20, 2002
**Date of Patent:** February 26, 2008
**Assignee:** Altera Corporation
**Inventors:** Neil Mammen, Sagar Edara, Mammen Thomas, Greg Maturi

### ADAPTING VIDEO IMAGES FOR WEARABLE DEVICES

**Publication number:** 20180295352

**Abstract:** A spatial direction of a wearable device that represents an actual viewing direction of the wearable device is determined. The spatial direction of the wearable device is used to select, from a multi-view image comprising single-view images, a set of single-view images. A display image is caused to be rendered on a device display of the wearable device. The display image represents a single-view image as viewed from the actual viewing direction of the wearable device. The display image is constructed based on the spatial direction of the wearable device and the set of single-view images.
**Type:** Application
**Filed:** April 10, 2018
**Publication date:** October 11, 2018
**Applicant:** Dolby Laboratories Licensing Corporation
**Inventors:** Ajit NINAN, Neil Mammen

### Passive Multi-Wearable-Devices Tracking

**Publication number:** 20180293752
**Abstract:** At a first time point, a first light capturing device at a first spatial location in a three-dimensional (3D) space captures first light rays from light sources located at designated spatial locations on a viewer device in the 3D space. At the first time point, a second light capturing device at a second spatial location in the 3D space captures second light rays from the light sources located at the designated spatial locations on the viewer device in the 3D space. Based on the first light rays captured by the first light capturing device and the second light rays captured by the second light capturing device, at least one of a spatial position and a spatial direction, at the first time point, of the viewer device is determined.
**Type:** Application
**Filed:** April 10, 2018
**Publication date:** October 11, 2018
**Applicant:** Dolby Laboratories Licensing Corporation
**Inventors:** Ajit NINAN, Neil MAMMEN

### AUGMENTED 3D ENTERTAINMENT SYSTEMS

**Publication number:** 20180295351
**Abstract:** A wearable device comprises a left view optical stack for a viewer to view left view cinema display images rendered on a cinema display and a right view optical stack for the viewer to view right view cinema display images rendered on the cinema display. The left view cinema display images and the right view cinema display images form stereoscopic cinema images. The wearable device further comprises a left view imager that renders left view device display images, to the viewer, on a device display, and a right view imager that renders right view device display images, to the viewer, on the device display. The left view device display images and the right view device display images form stereoscopic device images complementary to the stereoscopic cinema images.
**Type:** Application
**Filed:** April 4, 2018
**Publication date:** October 11, 2018
**Applicant:** Dolby Laboratories Licensing Corporation
**Inventors:** Ajit NINAN, Neil MAMMEN

### Method and apparatus for packet segmentation, enqueuing and queue servicing for multiple network processor architecture

**Patent number:** 7320037
**Abstract:** A method is described that forms different pieces of a packet and sends each one of the pieces toward a different memory unit amongst a plurality of memory units. Each one of the memory

units is managed by a different network processor. The method also receives each of the different pieces, each of the pieces having been read from its respective memory unit of the plurality of memory units.
**Type:** Grant
**Filed:** May 10, 2002
**Date of Patent:** January 15, 2008
**Assignee:** Altera Corporation
**Inventors:** Greg Maturi, Sager Edara, Neil Mammen

### Packet classification method

**Patent number:** 7277437
**Abstract:** According to one embodiment, a network hardware machine is disclosed. The network hardware machine includes a central processing unit (CPU) that processes data packets received at the network hardware machine, and a classifier, coupled to the CPU, that classifies the packets prior to the packets being received at the CPU.
**Type:** Grant
**Filed:** May 20, 2002
**Date of Patent:** October 2, 2007
**Assignee:** Altera Corporation
**Inventors:** Neil Mammen, Mammen Thomas, Sanjay Agarwal, M. Varghese Ninan

### Method and apparatus for a network processor having an architecture that supports burst writes and/or reads

**Patent number:** 7206857
**Abstract:** A method is described that involves recognizing that an input queue state has reached a buffer's worth of information. The method also involves generating a first request to read a buffer's worth of information from an input RAM that implements the input queue. The method further involves recognizing that an output queue has room to receive information and that an intermediate queue that provides information to the output queue does not have information waiting to be forwarded to the output queue. The method also involves generating a second request to read information from the input RAM so that at least a portion of the room can be filled. The method also involves granting one of the first and second requests.
**Type:** Grant
**Filed:** May 10, 2002
**Date of Patent:** April 17, 2007
**Assignee:** Altera Corporation
**Inventors:** Neil Mammen, Greg Maturi, Mammen Thomas

### Detecting bit errors in a communications system

**Patent number:** 6983403
**Abstract:** Error codes output from a serializer/deserializer in a node of a communications network are detected by error decode logic that assumes that each new error occurrence reflects a one bit error in the word giving rise to the error code. Each error occurrence is then counted. When the error count reaches a predetermined limit (e.g., 250 errors), the total bit count required to accumulate the 250 errors is then determined. The total bits can be determined based on a clock count (time). The BER is then calculated based upon the fixed error limit and the total bit count. This BER is then reported and used to determine the health of the network.
**Type:** Grant
**Filed:** March 2, 2001
**Date of Patent:** January 3, 2006
**Assignee:** Luminous Networks, Inc.

**Inventors:** Derek Mayweather, Steven Gemelos, Neil Mammen, Jason Fan

**Business method for selling advertisements and traffic related services on electronic billboards**

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